

Response After Final  
Application No. 10/648,283  
Attorney Docket No. 031080

**REMARKS**

Claim 1-22 are pending in the present application. By this Amendment, claims 1, 4, 5, 6, 12, 16 and 18 have been amended and claim 2 has been cancelled. No new matter has been added. It is respectfully submitted that this Amendment is fully responsive to the Office Action dated August 4, 2006.

**35 USC §112, Second Paragraph Rejection:**

Claims 1-22 stand rejected under §112, second paragraph, as being indefinite for failing to particularly point out and distinctly point out the subject matter which applicant regards as the invention.

This rejection is respectfully traversed.

It is respectfully submitted that the amendments made to independent claims 1, 16 and 18 overcome this rejection. Accordingly, withdrawal of this rejection is respectfully requested.

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**As to the Merits:**

As to the merits of this case, the Examiner maintains the following rejections:

- 1) claims 1-2, 14 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Hamase (JP Pub No. 2002135095);
- 2) claims 3, 11 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamase (JP Pub No. 2002135095).
- 3) claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamase (JP Pub No. 2002135095) in view of Yoshida et al. (U.S. Pat. No. 4,317,055).
- 4) claims 5, 7-9, 13 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamase (JP Pub No. 2002135095) in view of Matsunaga et al. (U.S. Pub. No. 0030016082).
- 5) claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamase (JP Pub No. 2002135095) in view of Ayasli et al. (U.S. Pat. No. 5,012,123).
- 6) claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamase (JP Pub No. 2002135095) in view of Ayasli et al. (U.S. Pat. No. 5,012,123).

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Each of these rejections is respectfully traversed.

Claim 1, as amended, now calls *switching transistors commonly connected to a connection node; and a control bias supply circuit that supplies a control bias for cutting off all the switching transistors to the switching transistors in order to prevent high frequency signal from substantially propagating through all the switching transistors when all of the switching transistors are in a non-selected state in which all the switching transistors are turned OFF in response to selection control signals applied thereto*. Independent claims 16 and 18 include similar features.

For example, according to the switching circuit shown in Fig. 3 of the present application, there is provided a switching circuit comprising the switching transistors (T1, T2) commonly connected to a connection node (Ps); and a control bias supply circuit (10) that supplies a control bias for cutting off all the switching transistors (T1, T2) to the switching transistors (T1, T2) in order to prevent a high frequency signal from substantially propagating through all the switching transistors (T1, T2) when all of the switching transistors (T1, T2) are in a non-selected state in which all the switching transistors are turned OFF in response to selection control signals (V1, V2) applied thereto.

In contrast, Hamase fails to teach or suggest such features as now called for in amended claim 1. That is, Hamase does not have any control bias supply circuit as required in amended

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claim 1. The Examiner stated that the resistor circuitry corresponds to the control bias supply circuit. However, the resistor circuitry supplies the transistors with selection control signals for turning ON/OFF these transistors.

That is, it is noted that in the present claimed invention the control bias supply circuit supplies the connection node with a control bias that is provided separate for the selection control signals and is used for cutting off all the transistors.

It is submitted that this kind of control bias supply circuit is not provided in Hamase.

Accordingly, it is submitted that Hamase fails to disclose or fairly suggest the features of claim 1 concerning *switching transistors commonly connected to a connection node; and a control bias supply circuit that supplies a control bias for cutting off all the switching transistors to the switching transistors in order to prevent high frequency signal from substantially propagating through all the switching transistors when all of the switching transistors are in a non-selected state in which all the switching transistors are turned OFF in response to selection control signals applied thereto.*

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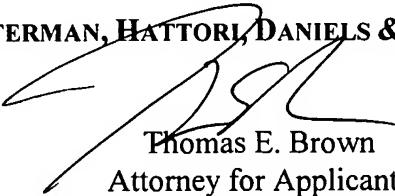
In view of the aforementioned amendments and accompanying remarks, Applicants submit that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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